Examiner's amendment

1. (Currently amended) An equalizer circuit comprising:

carrier sensing means for sensing a ~~the~~ start of a reception of a signal on the basis of a signal representing a reception level of the reception signal and outputting a detection signal;

first and second equalizing means for equalizing the reception signal, said reception signal being simultaneously fed to each of said first and second equalizing means;

control means for alternately enabling said first and second equalizing means every frame reception in accordance with said detection signal output from said carrier sensing means, said control means including a carrier sense controller for generating first and second carrier sense signals and first and second gate circuits receiving said first and second carrier sense signals respectively, each of said first and second gate circuits receiving a clock signal;

and

switching means for alternately switching between outputs from said first and second equalizing means every frame reception and outputting a ~~the~~ selected output of one of said first and second equalizing means as demodulation data.

2. (Currently amended) ~~A~~ An equalizer circuit according to claim 1, wherein said control means alternately outputs said first and second carrier sense signals to said first and second equalizing means from a time when the detection signal is output from said carrier sensing means to a time when

equalizing processing is complete in said first and second equalizing means,

and

said first and second equalizing means alternately equalize the reception signal every frame reception in response to said first and second carrier sense signals from said control means.

4 8. (Currently amended) An equalizer circuit comprising:

carrier sensing means for sensing a ~~the~~ start of a reception of a signal on the basis of a signal representing a reception level of the reception signal and outputting a detection signal;

first and second equalizing means for equalizing the reception signal;

control means for alternately enabling said first and second equalizing means every frame reception in accordance with said detection signal output from said carrier sensing means; and

switching means for alternately switching between outputs from said first and second equalizing means every frame reception and outputting ~~the~~ a selected output of one of said first and second equalizing means as demodulation data;

wherein said control means alternately outputs first and second carrier sense signals to said first and second equalizing means from a time when the reception signal is output from said carrier sensing means to a time when equalizing processing is complete in said first and second equalizing means, and

wherein said first and second equalizing means alternately equalize the reception signal every frame reception in response to said first and second carrier sense signals from said control means;

said equalizer circuit further comprising first and second gate means for receiving a system clock signal and the first and second carrier sense signals from said control means and supplying an output clock signal to said first and second equalizing means.

6 4. (Currently amended) An equalizer circuit comprising:

carrier sensing means for sensing a ~~the~~ start of a reception of a signal on the basis of a signal representing a reception level of the reception signal and outputting a detection signal;

first and second equalizing means for equalizing the reception signal;

control means for alternately enabling said first and second equalizing means every frame reception in accordance with said detection signal output from said carrier sensing means; and

switching means for alternately switching between outputs from said first and second equalizing means every frame reception and outputting ~~the~~ a selected output of one of said first and second equalizing means as demodulation data;

wherein:

said control means alternately outputs first and second carrier sense signals to said first and second equalizing means from a time when the reception signal is output from said carrier sensing means to a time when equalizing processing is complete in said first and second equalizing means;

said first and second equalizing means alternately equalize the reception signal every frame reception in response to said first and second carrier sense signals from said control means

said first and second equalizing means output first and second demodulation data used

during equalizing processing to said switching means and output first and second demodulation data gate signals synchronized with the first and second demodulation data to said control means and said switching means,

said control means stops outputting the first and second carrier sense signals in response to the first and second demodulation data gate signals, and

said switching means alternately outputs the first and second demodulation data in response to the first and second demodulation data gate signals.

3 5. (Currently Amended) ~~A~~ An equalizer circuit according to claim 2, wherein

said first and second equalizing means comprise equalizers for setting tap coefficients and memories for storing preamble signals of the reception signal, and

said first and second equalizing means detect frequency offset values, estimate transmission line characteristics, and set the tap coefficients at the start of reception of the reception signal.

8 6. (Currently amended) An equalizing method comprising:

detecting ~~the~~ a start of a reception signal on the basis of a signal representing a reception level of the reception signal;

simultaneously feeding said reception signal to first and second equalizer units;

alternately enabling said first and second equalizer units for equalizing the reception signal upon detecting the start of the reception signal, said enabling including: (1) generating first and second carrier sense signals and feeding ~~same~~ said first and second carrier sense signals to said first and second equalizer units and (2) gating a

clock signal and said first and second carrier sense signals and supplying an output clock signal to said first and second equalizer units; and

alternately switching between outputs from said first and second equalizer units every frame reception and outputting ~~the~~ a selected output of one of said first and second equalizing means as demodulation data.

9 X (Currently amended) An equalizing method according to claim ~~6~~ 8, wherein enabling further comprises alternately outputting the first and second carrier sense signals ~~enabling~~ to enable said first and second equalizer units for a time interval from a time when the start of the reception signal is detected to a time when equalizing processing is complete in said first and second equalizer units.

11 X (Currently amended) An equalizing method comprising:

detecting ~~the~~ a start of a reception signal on the basis of a signal representing a reception level of the reception signal;

simultaneously feeding said reception signal to first and second equalizer units;

alternately enabling said first and second equalizer units for performing equalizing processing of the reception signal upon detecting the start of the reception signal, said enabling including: (1) alternately generating first and second carrier sense signals and feeding ~~same~~ the first and second carrier sense signals to said first and second equalizer units and (2) gating a clock signal to said first and second equalizer units;

alternately switching between outputs from said first and second equalizer units every frame reception and outputting ~~the~~ a selected output of one of said first and second equalizing means as demodulation data, said first and second carrier sense signals enabling said first and second equalizer units for a time interval from a time when the start of the reception signal is detected to a time when said equalizing processing is complete in said first and second equalizer units; and

alternately supplying said clock signal to said first and second equalizer units in accordance with the first and second carrier sense signals.

12 9. (Currently amended) ~~The~~ An equalizing method as recited in claim 11 further comprising:

alternately outputting first and second demodulation data used during the equalizing processing in response to first and second demodulation data gate signals produced by said first and second equalizer units respectively.

5 10. (Currently amended) An equalizer circuit according to claim 4, wherein said first and second equalizing means comprise equalizers for setting tap coefficients and memories for storing preamble signals of the reception signal, and said first and second equalizing means detect frequency offset values, estimate transmission line characteristics, and set the tap coefficients at the start of reception of the reception signal.

7 11. (Currently amended) An equalizer circuit according to claim 6, wherein said first and second equalizing means comprise equalizers for setting tap coefficients and memories for storing preamble signals of the reception signal, and

said first and second equalizing means detect frequency offset values, estimate

transmission line characteristics, and set the tap coefficients at the start of reception of the reception signal.

10 12. (Currently amended) An equalizing method according to claim 8, wherein:

said first and second ~~equalizing~~ equalizer units comprise equalizers for setting tap coefficients and memories for storing preamble signals of the reception signal, and

said first and second ~~equalizing~~ equalizer units detect frequency offset values, estimate transmission line characteristics, and set the tap coefficients at the start of reception of the reception signal.

14 13. (Currently amended) An equalizing method according to claim 11, wherein:

said first and second ~~equalizing~~ equalizer units comprise equalizers for setting tap coefficients and memories for storing preamble signals of the reception signal, and

said first and second ~~equalizing~~ equalizer units detect frequency offset values, estimate transmission line characteristics, and set the tap coefficients at the start of reception of the reception signal.

13 14. (Currently amended) An equalizing method according to claim 12, wherein:

said first and second ~~equalizing~~ equalizer units comprise equalizers for setting tap coefficients and memories for storing preamble signals of the reception signal, and

said first and second ~~equalizing~~ equalizer units detect frequency offset values, estimate transmission line characteristics, and set the tap coefficients at the start of reception of the reception signal.